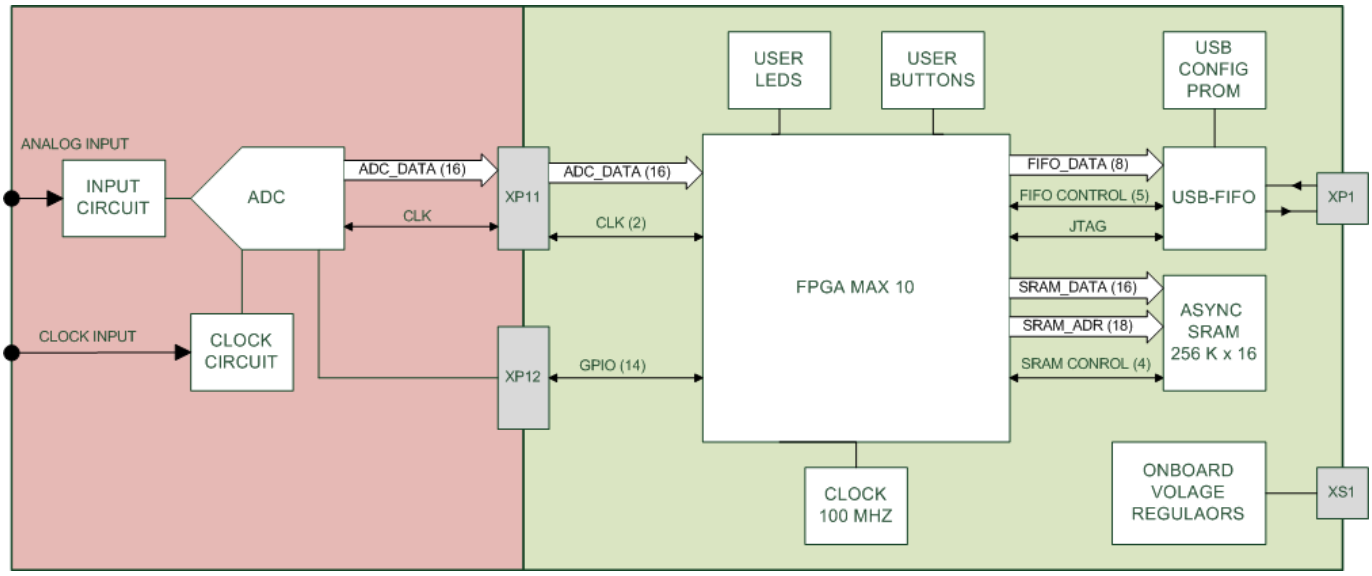
Thesys-Intechna

High Speed ADC Data Capture Board

DATASHEET TI-DAB-16/100M

FUNCTIONAL BLOCK DIAGRAM



FEATURES

- Intel MAX 10 FPGA for digital data capturing and ADC control
- 512 KB SRAM memory for ADC data storage
- 16-bit parallel data input bus supporting ADCs with sample rate of up to 100 MSPS
- CMOS interface with voltages: 1.8, 2.5, 3.3, 5 V
- USB-FIFO bridge for data transferring to PC at speed of 320 Mb/s (USB 2.0 interface)
- Reconfiguration of the FPGA via USB interface with the built-in programmer
- Compatibility of the programmer with the Intel software component
- On-board clock generator
- Powered by PC USB port or external DC 5 V supply 0.5 A

APPLICATIONS

- Measurements of static characteristics of ADCs (INL, DNL, OE, GE)
- Measurements of dynamic characteristics of ADCs (SNR, SINAD, SFDR, THD, ENOB)
- Collection and processing of digital data
- Measuring stands control

REQUIRED EQUIPMENT

- ADC Evaluation Board, compatible with this data capture board
- Personal computer with Windows 7 or Windows 8.1 operating system
- Software for the selected ADC chip
- USB-A-USB-B cable for connecting data capture boards to PC

LIST OF CONTENTS

DATA CAPTURE BOARD DEVICE

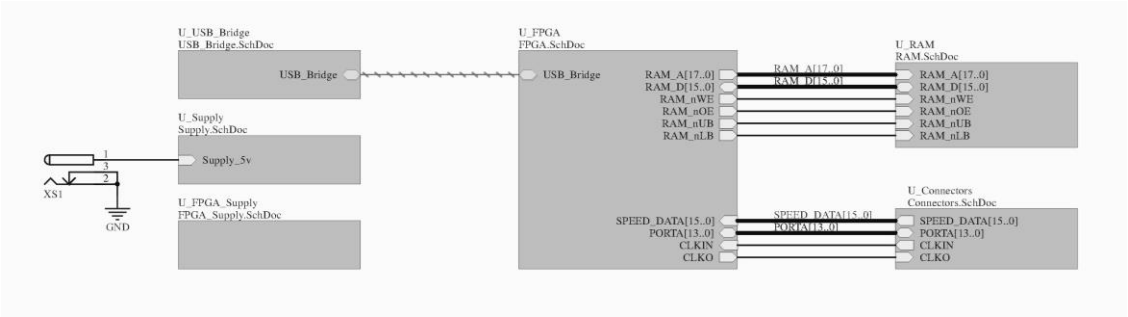


Figure 1. Block diagram of the data capture board

This product is designed for high-speed data capturing from measured ADC chips and is used with the program for a personal computer. The data capture board is connected to a PC via the USB interface. The hardware complex has the FPGA unit for rapid reconfiguration of the system for various measurements modes and the SRAM unit for storing of sampled data obtained during measurements.

The TI-DAB-16/100M data capture board uses the FPGA chip of the MAX10 series (10M50SAE144C8GES) as the main control component. The FPGA is configured for ADCs static and dynamic characteristics tests. Data collected during measurements is transmitted to a PC via the USB-bridge FT2232HL.

Connection of the data capture board with an evaluation board of an ADC is held with XP11 and XP12 connectors. The data capture board has the clock output for the evaluation board of an ADC (CLKO) and the synchronization input (CLKI). The output Port A (PORTA) is used for generation of ADC control signals. Its operating mode depends on the selected ADC debug card. The input data bus SPEED_DATA is used for collection of the data coming from an ADC chip. Also, there implemented the SPI Master interface in the FPGA chip for operation with the configurable periphery, which is located on the evaluation board of an ADC. Voltages of the digital inputs/outputs of the FPGA chip can be set with the V_SEL jumper block (table 3).

For dynamic tests, the data acquisition board includes the IS61WV25616BLL-10TLI memory chip. During dynamic measurements, test sample of data is stored in the memory chip, and further is read and transmitted to a computer via the USB interface.

Note: To exchange information with a personal computer, the data collection board uses the FTDI USB-bridge chip. For correct operation of the measuring system, it is necessary to install on the computer the D2XX driver for Windows.

COMPATIBILITY WITH OTHER PRODUCTS

TI-EAB-10/12b

BOARD FUNCTIONALITY

Firstly, the the data capture board is designed to measure static and dynamic characteristics of ADCs.

Jumper blocks and buttons located on the board are the Controls of a measurement process. To restart a test stand in case of a malfunction, use the SA1 and SA7 buttons with the RESET caption.

Blinking LED0 (HL3) indicates the readiness of the data capture board for operation. To enable the indication, it is needed to to set LED0 (HL3) jumper in the jumper block XP8.

OPERATION WITH MEASURING SYSTEM

Required equipment:

- ADC Evaluation Board, compatible with this data capture board
- Personal computer with Windows 7 or Windows 8.1 operating system
- Software for a selected ADC chip
- USB-A-USB-B cable for connecting data capture boards to a PC

Note: Administrator rights are required for working with the measurement software.

MEASURING COMPLEX ADJUSTMENT

1. Set the needed operation mode of the data capture board using jumpers (see Jumper Blocks section).
2. Install software for a tested ADC chip on a personal computer.
3. Connect an ADC evaluation board to the data capture board.
4. Connect the data capture board and your personal computer with a USB-A-USB-B cable.
5. Connect the ADC evaluation board to a DC voltage source.
6. Configure the ADC evaluation board according to its technical description.
7. Run the software for the ADC chip and configure it according to the instructions.

JUMPER BLOCKS

Table 1. Selection of a power supply for the data capture board

XP3	Pin 1 to Pin 2	Board power through XS1 connector
XP3	Pin 3 to Pin 2	Board power through USB connector

Table 2. Power-off: IMEAS

XP4	on	Main power-on
XP4	off	Main power-off

Table 3. Selection of power supply voltages for digital inputs/outputs of the board: V_SEL

XP10	Pin 1 to Pin 2	+5V
XP10	Pin 3 to Pin 4	+3V3
XP10	Pin 5 to Pin 6	+2V5
XP10	Pin 7 to Pin 8	+1V8
XP10	Pin 9 и Pin 10	ADJ

Table 4. Selection of USB-bridge operation mode: PWREN #

XP2	on	Bridge in not active state
XP2	off	Bridge in active state

Table 5. Connection of LEDs located on board to PORTB [0..5]: LEDS

XP8	Pin 3 to Pin 4	LED5 is connected
XP8	Pin 5 to Pin 6	LED4 is connected
XP8	Pin 7 to Pin 8	LED3 is connected
XP8	Pin 9 to Pin 10	LED2 is connected
XP8	Pin 11 to Pin 12	LED1 is connected
XP8	Pin 13 to Pin 14	LED0 is connected

BOARD POWER SUPPLY VOLTAGE CONTROL

USB-A socket is used to power the board by default and is set by XP3 jumper. If output current/voltage of the USB port doesn't meet the requirement of 5V/0.5A, an external power supply that meets the stated requirement can be used to power the board by connecting it to the XS1 connector and switching on the power supply from the external power supply by the XP3 jumper.

Jumper IMEAS (XP4) can be used for extreme shutdown of the board or for its current consumption measuring.

CONNECTION WITH EVALUATION BOARD INTERFACE

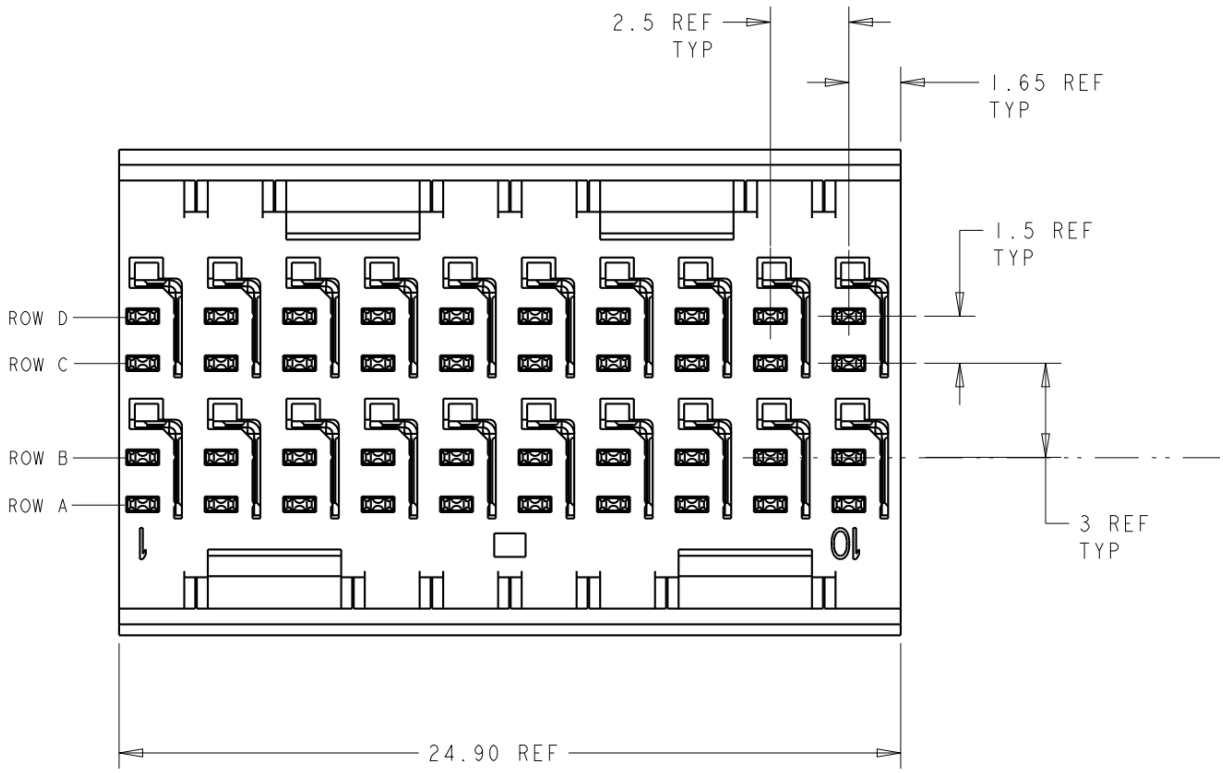


Figure 2. Drawing of 6469169-1 connector

Two 6469169-1 connectors located on the edge of the board (XP11, XP12) are used to connect the data capture board with an evaluation board of the ADC. I / O ports are connected through these connectors, as shown in tables 6-7.

Table 6. I/O connector — XP11 pin mapping

Connector	Contact	Function
XP11	B1	Speed_Data_1
XP11	B2	Speed_Data_3
XP11	B3	Speed_Data_5
XP11	B4	Speed_Data_6
XP11	B5	Speed_Data_7
XP11	B6	Speed_Data_9
XP11	B7	Speed_Data_11
XP11	B8	Speed_Data_13
XP11	B9	GND
XP11	B10	GND
XP11	D1	Speed_Data_0
XP11	D2	Speed_Data_2
XP11	D3	Speed_Data_4
XP11	D4	CLKO
XP11	D5	CLKI
XP11	D6	Speed_Data_8
XP11	D7	Speed_Data_10
XP11	D8	Speed_Data_12
XP11	D9	Speed_Data_14
XP11	D10	Speed_Data_15
XP11	A1	GND
XP11	A2	GND
XP11	A3	GND
XP11	A4	GND
XP11	A5	GND
XP11	A6	GND
XP11	A7	GND
XP11	A8	GND
XP11	A9	GND
XP11	A10	GND
XP11	C1	GND
XP11	C2	GND
XP11	C3	GND
XP11	C4	GND
XP11	C5	GND
XP11	C6	GND
XP11	C7	GND
XP11	C8	GND
XP11	C9	GND
XP11	C10	GND

Table 7. I/O connector — XP12 pin mapping

Connector	Contact	Function
XP12	B1	Device_1_nCS
XP12	B2	Device_1_MOSI
XP12	B3	Device_1_SCLK
XP12	B4	NC
XP12	B5	Device_2_nCS
XP12	B6	Device_2_MOSI
XP12	B7	Device_2_SCLK
XP12	B8	GND
XP12	B9	GND
XP12	B10	GND
XP12	D1	PORTA0
XP12	D2	PORTA2
XP12	D3	PORTA4
XP12	D4	PORTA6
XP12	D5	PORTA8
XP12	D6	PORTA10
XP12	D7	PORTA12
XP12	D8	GND
XP12	D9	GND
XP12	D10	GND
XP12	A1	GND
XP12	A2	GND
XP12	A3	GND
XP12	A4	GND
XP12	A5	GND
XP12	A6	GND
XP12	A7	GND
XP12	A8	GND
XP12	A9	GND
XP12	A10	GND
XP12	C1	GND
XP12	C2	GND
XP12	C3	GND
XP12	C4	GND
XP12	C5	GND
XP12	C6	GND
XP12	C7	GND
XP12	C8	GND
XP12	C9	GND
XP12	C10	GND

The high-speed I/O port SPEED_DATA is configured depending on the selected ADC chip. It also has a clock output and a clock input.

The high-speed I/O port PORTA is configured depending on the selected ADC chip. It has two SPI interfaces in Master mode, which can be used to control peripheral equipment located on an evaluation board of the ADC.

DATA CAPTURE BOARD SCHEMATICS

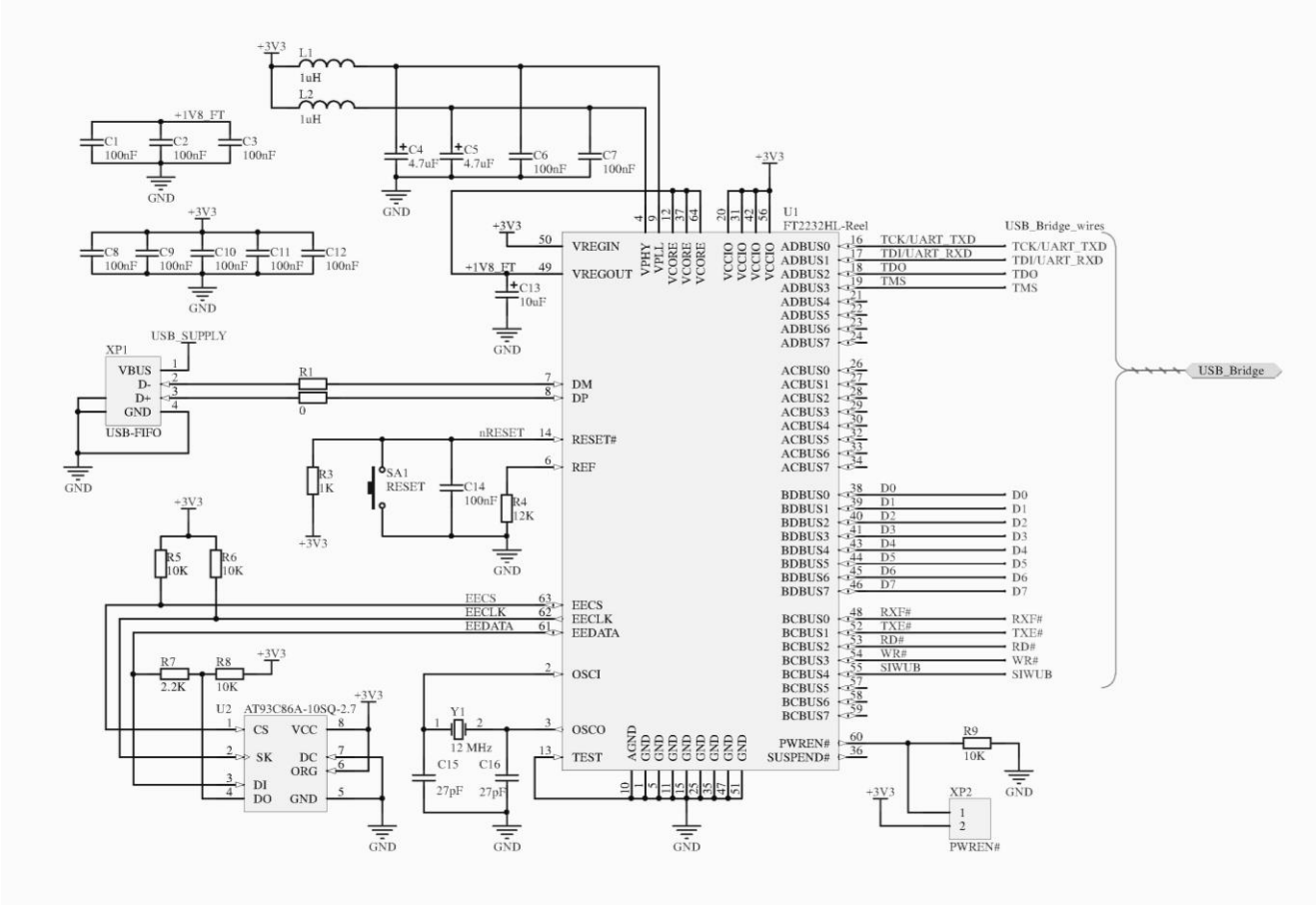


Figure 3. Schematic electrical diagram of the USB-bridge

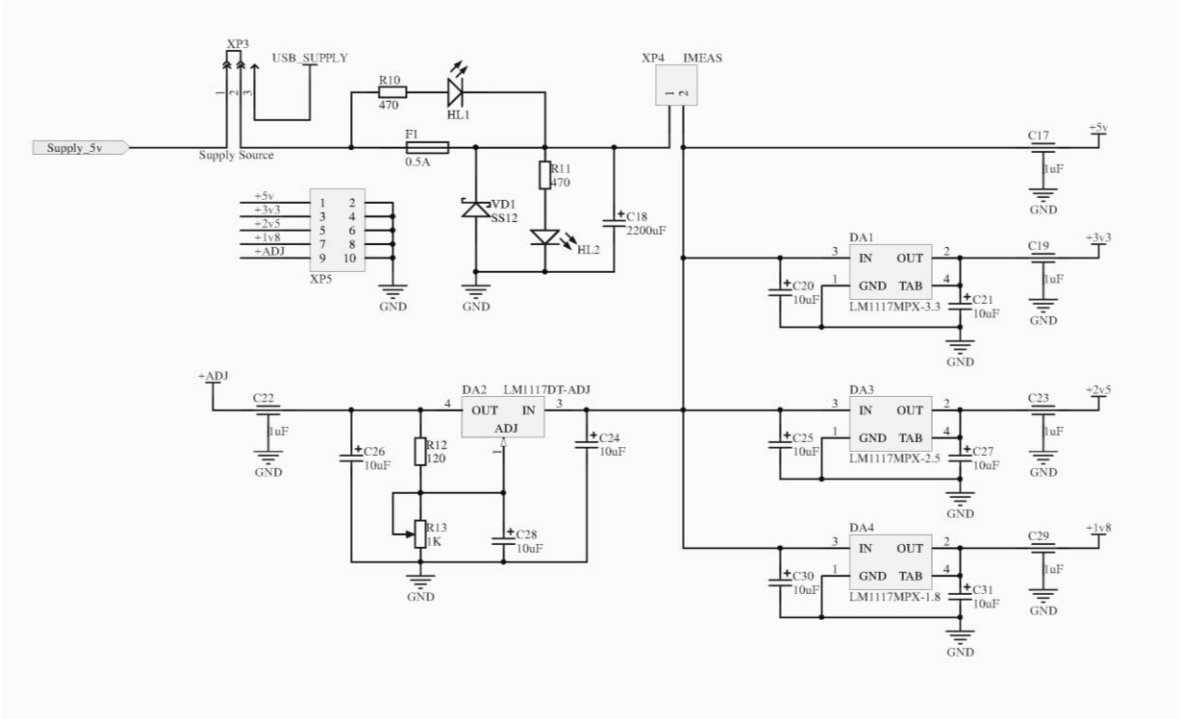


Figure 4. Schematic electrical diagram of the linear regulator block

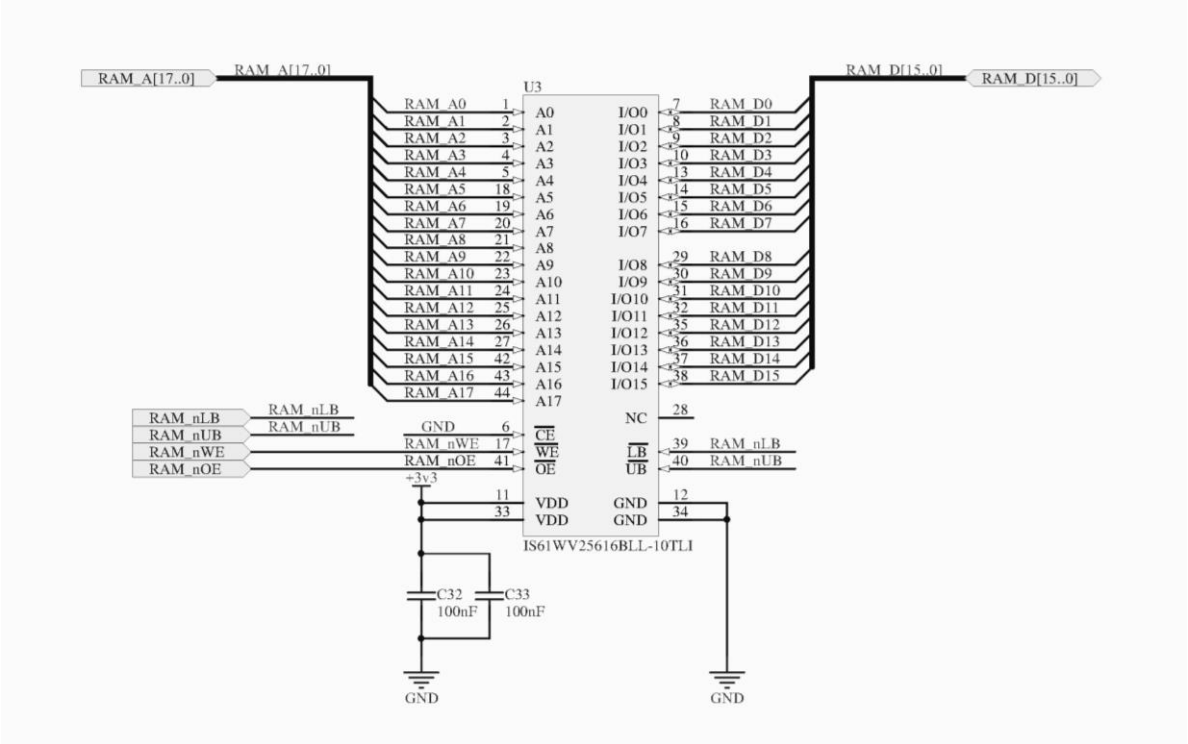


Figure 5. Schematic electrical diagram of the SRAM block

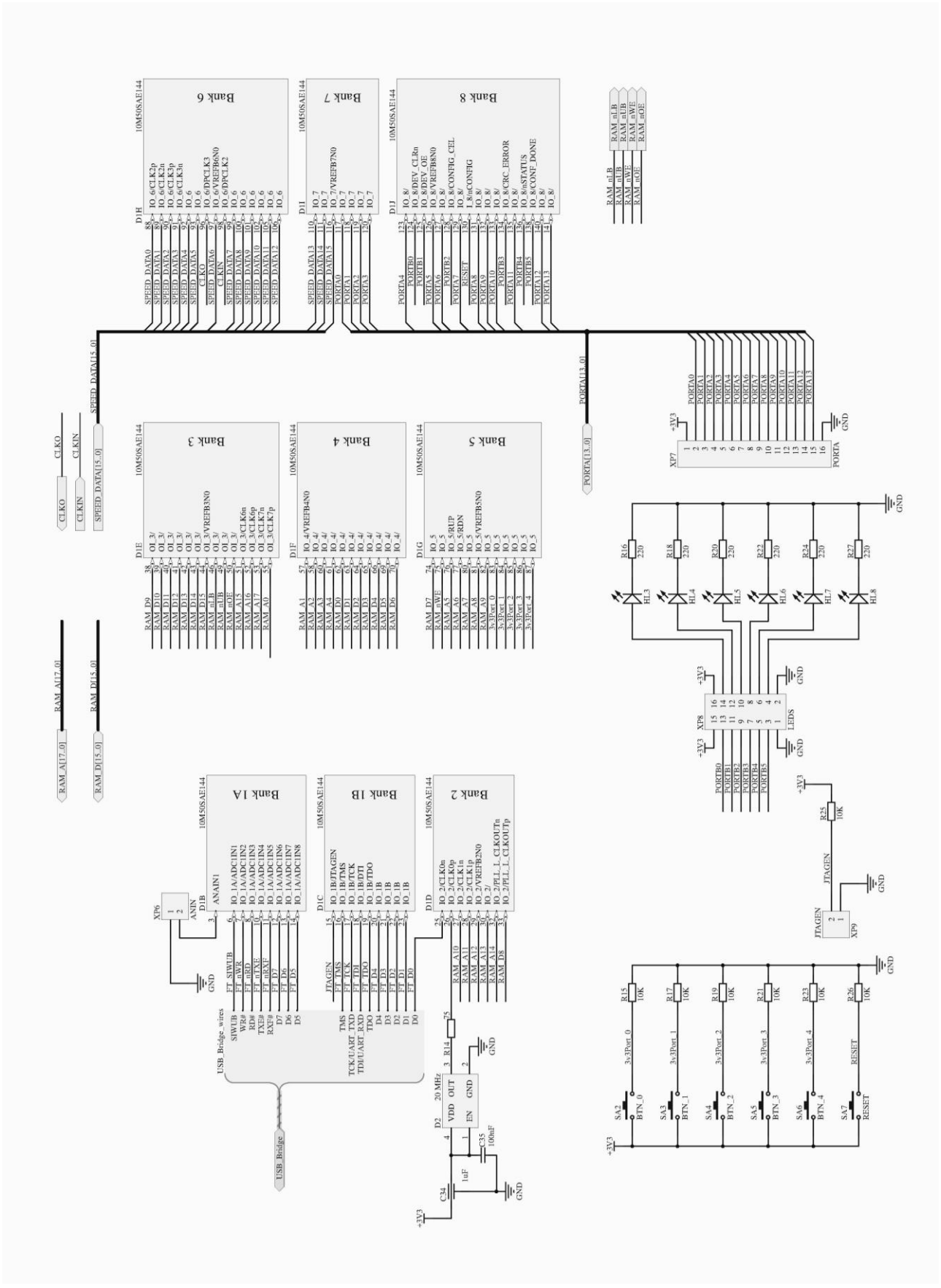


Figure 6. Schematic electrical diagram of the ports block

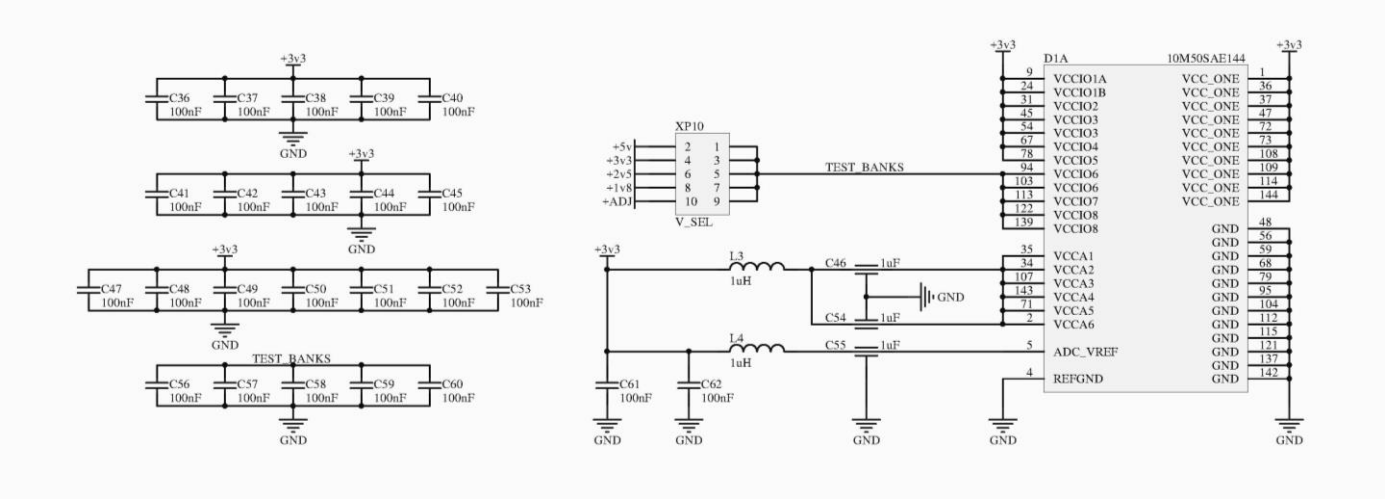


Figure 7. Schematic electrical diagram of the supply FPGA chips

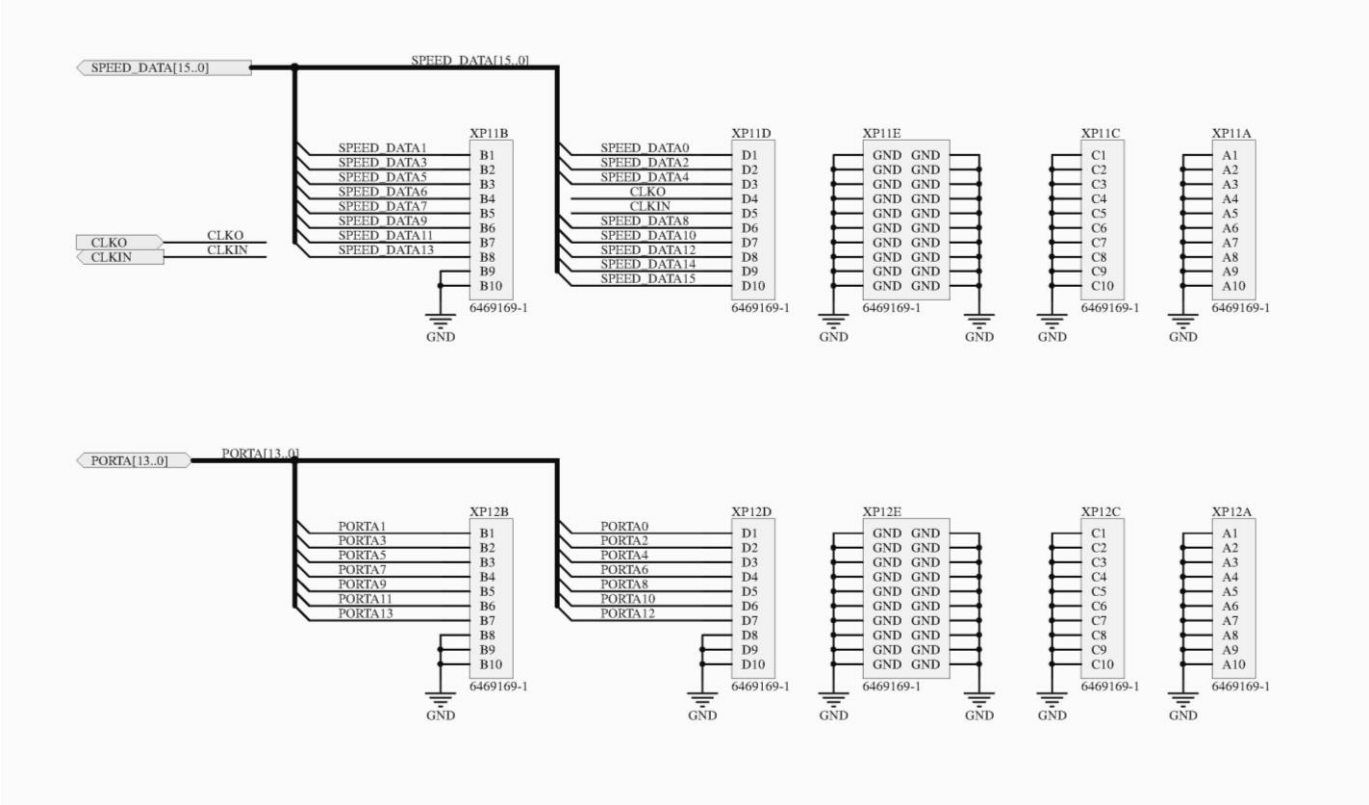


Figure 8. Schematic electrical diagram of the connectors

PCB LAYOUT

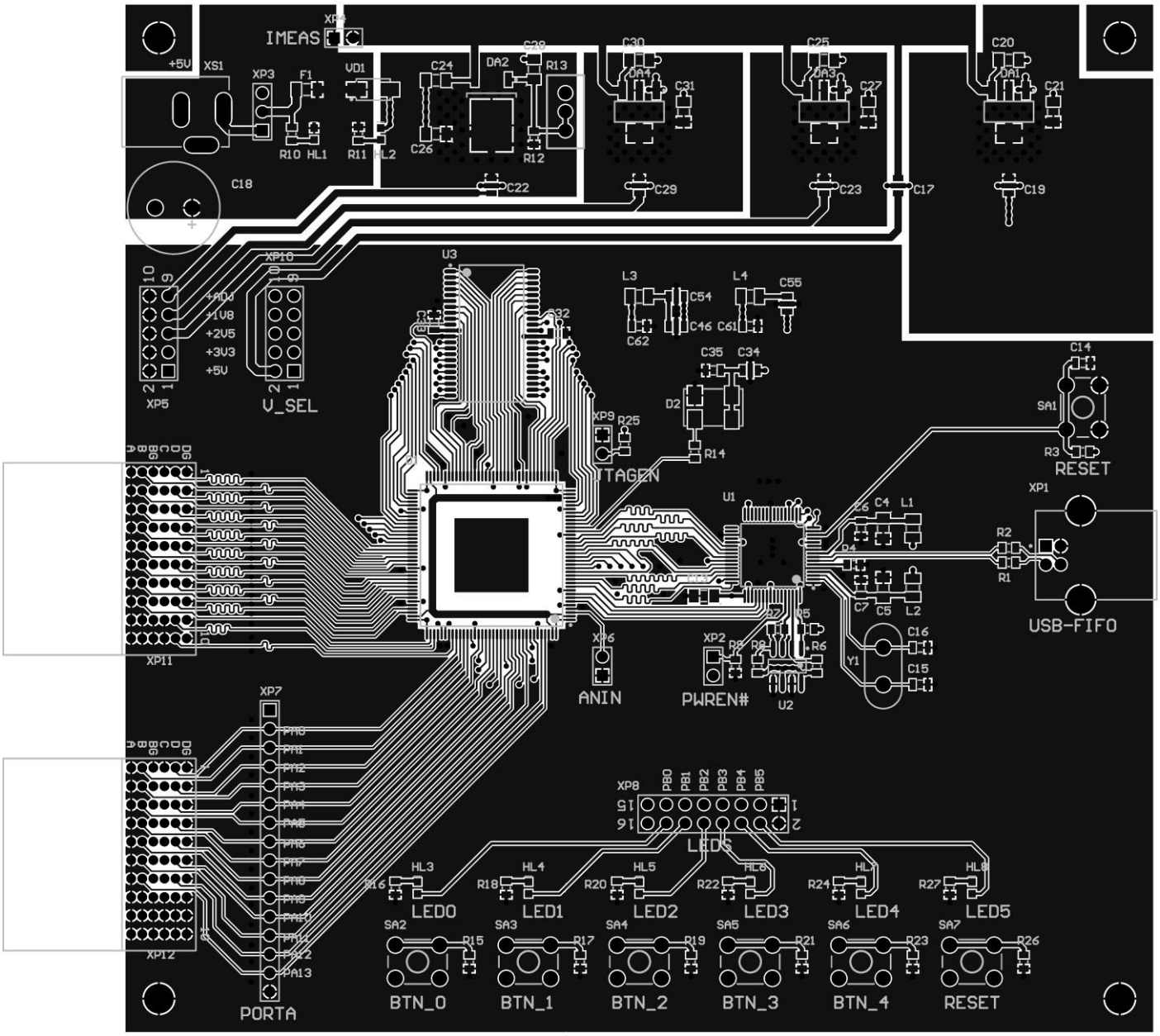


Figure 9. Drawing of the PCB top layer

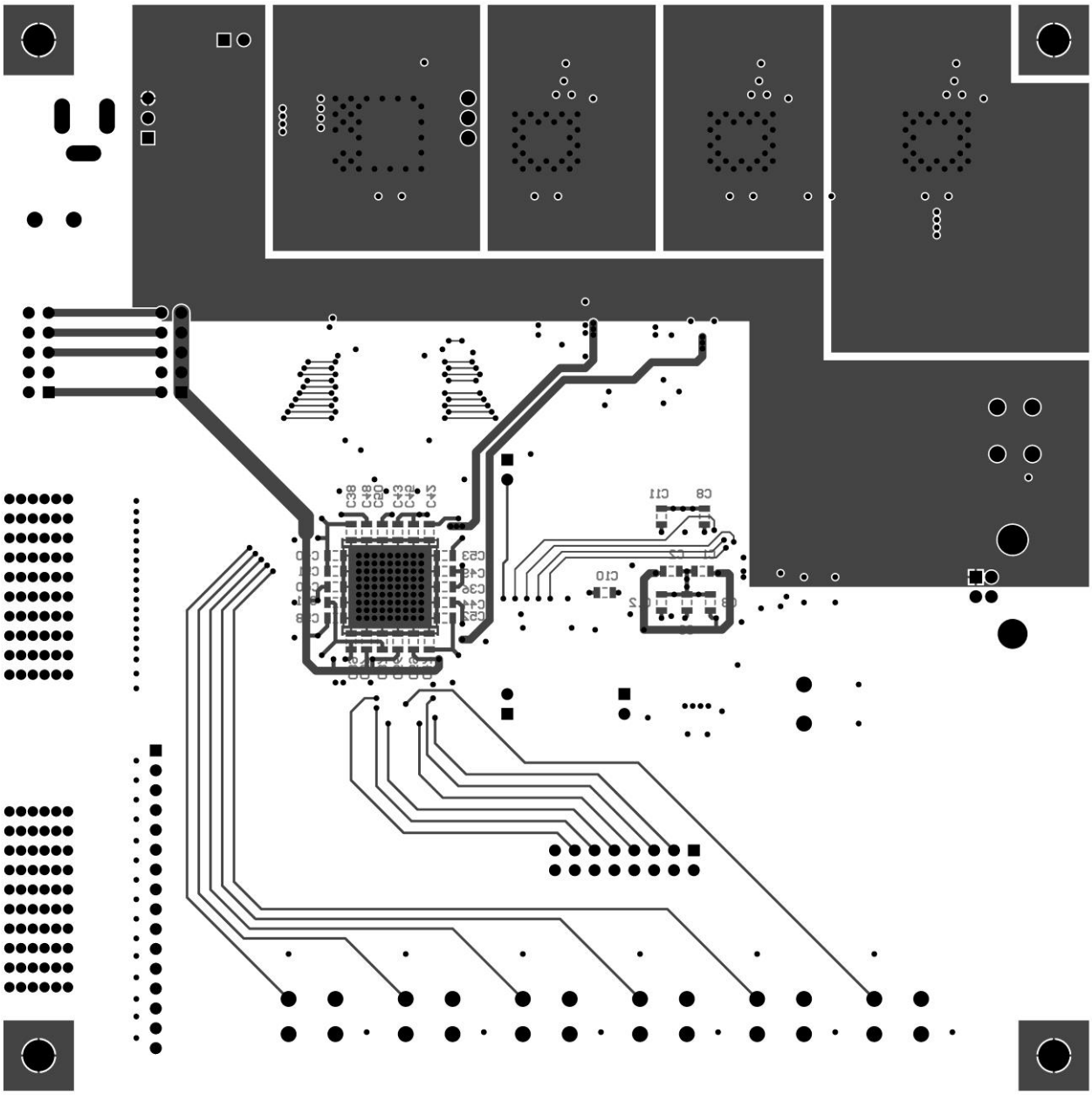


Figure 10. Drawing of the PCB bottom layer

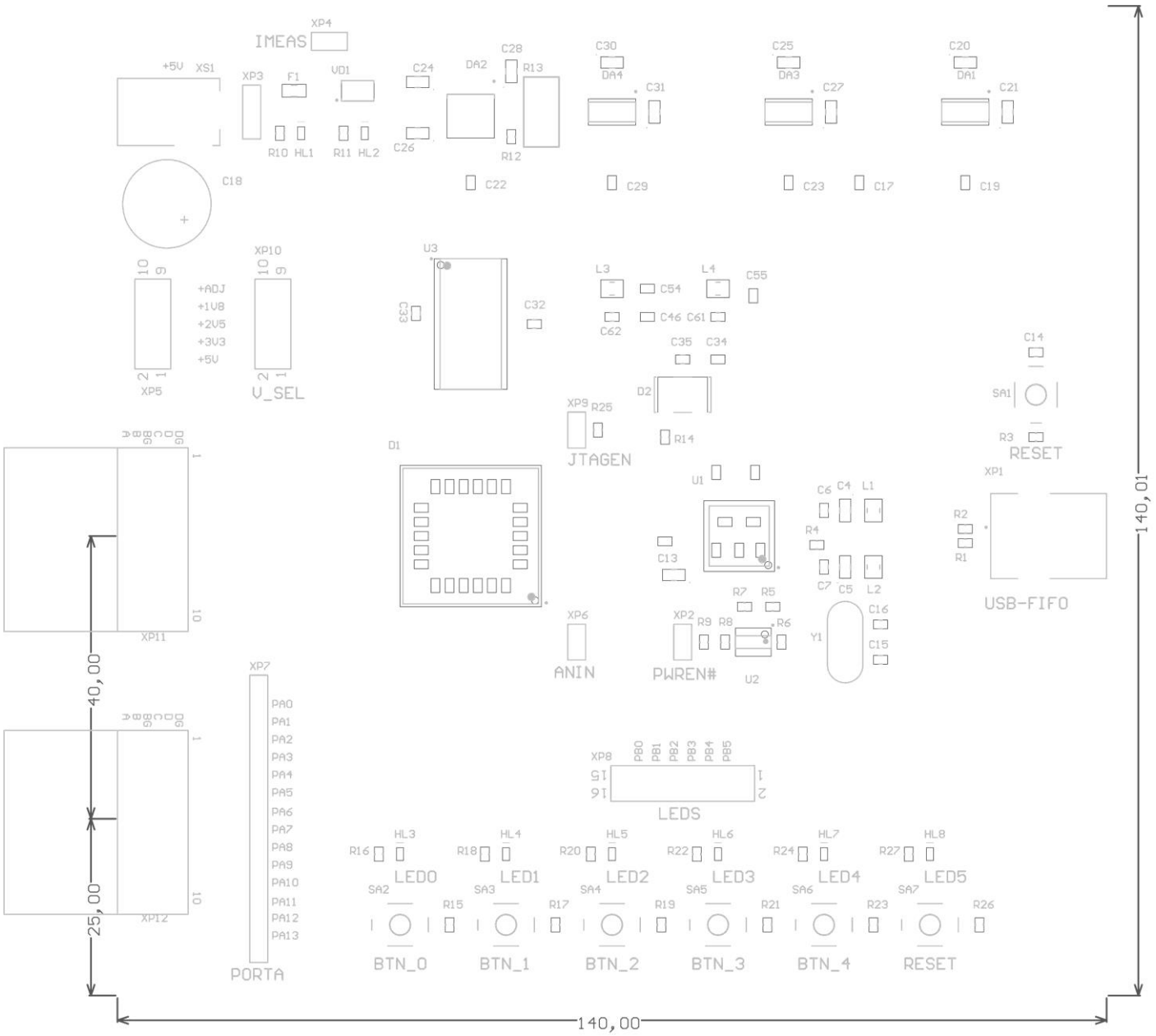


Figure 11. PCB assembly drawing